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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/738,099	12/15/2000	Samuel Alan Meddaugh	LMCO.04PA	9675

7590 01/14/2005
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EXAMINER

SHANNON, MICHAEL R

ART UNIT PAPER NUMBER

2614

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/738,099

Applicant(s)

MEDDAUGH ET AL.

Examiner

Michael R Shannon

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 December 2000.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☒ Claim(s) 11-17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Claim Objections

1. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 11-17 been renumbered 12-18, respectively.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 5, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamlin US patent 5,574,964, cited by examiner, in view of Filor et al US patent 5,844,609, cited by examiner.

Regarding claim 1, the claimed circuit arrangement for providing a video signal to a video display from a selectable subset of a plurality of digital video data carried on a plurality of video data channels, wherein the digital video data is generated from video signals from a plurality of video sources, and each video

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channel selectably carries either color or monochrome video data is met as follows:

Hamlin discloses all of the following:

- The claimed data processor configured and arranged to interpret display commands is met by the CPU 43 of the system controller [Fig. 3].
- The claimed selector circuit coupled to the processor and having a plurality of output ports and input ports arranged for connection to the plurality of video data channels, the selector circuit configured and arranged to select digital video data received at a first data rate from a subset of the channels responsive to an input selection signal from the processor and provide selected digital video data at the output ports at a second data rate that is half the first data rate is met by the converter 34 [Fig. 2], which serves to input a plurality of signals and convert them so as to make them accessible on communication bus 36.
- The claimed plurality of data routers, each having an output port and an input port coupled to a respective one of the output ports of the selector circuit, and each data router configured and arranged to convert input video data from YCrCb format to RGB format are met by the plurality of interface pods, which are coupled to the communication data bus 36 and serve to receive video content for display or use at the user location. The conversion from YCrCb to RGB format is not discussed in this source, however, is it disclosed in Filor (as will be discussed below).

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- The claimed video data sequencer coupled to the output ports of the data router, the sequencer configured and arranged to merge the selected video data into frames of video data is met by the Frequency Synthesizer 62 and the Controller/Demodulator 60, which both serve to sequence the content delivered on the bus into frames for conversion or viewing of analog output by the receiving unit 46.
- The claimed Digital-to-analog converter coupled to the video data sequencer, the converter configured and arranged to generate an analog video signal from the frames of video data is met by the Frequency Synthesizer 62 and the Voltage Controlled Oscillator 63, both of which serve to process digital input and output analog output to the receiving unit 46 [Fig. 4].

As is discussed above, Hamlin does not disclose the YCrCb to RGB format conversion within the data routers (interface pods).

Filor et al disclose a system that utilizes a CSC (color space conversion) from YCrCb to RGB for further processing of the video image [col. 14, lines 5-15].

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the conversion from YCrCb to RGB into the interface pods, in order to allow for further processing of the video signal and for more advanced options for customizing and processing the displayed signal.

Regarding claim 5, the claimed circuit arrangement being supported on a circuit board having connectors arranged for connecting to the video channels is met by New Computer Board 31 [Fig. 1], of Hamlin, which is used to connect the input video from the multiple providers to the system as discussed above in claim 1.

Regarding claim 13, the claimed method for providing a video signal to a video display from a selectable subset of a plurality of digital video data carried on a plurality of video data channels, wherein the digital video data is generated from video signals from a plurality of video sources, and each video channel selectably carries either color or monochrome video data is met as follows:

Hamlin discloses all of the following:

- The claimed step of interpreting display commands that select a subset of the video data is met by the use of CPU 43 of the system controller [Fig. 3].
- The claimed steps of receiving digital video data on the plurality video data channels at a first data rate and selecting digital video data from a subset of the channels responsive to the display commands and providing as output selected digital video data at the output ports at a second data rate that is half the first data rate are met by the use of converter 34 [Fig. 2], which serves to input a plurality of signals and convert them so as to make them accessible on communication bus 36.

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- The step of merging the selected video data into frames of video data is met by the use of Frequency Synthesizer 62 and the Controller/Demodulator 60, which both serve to sequence the content delivered on the bus into frames for conversion or viewing of analog output by the receiving unit 46.
- The claimed step of converting the video data to an analog video signal from the frames of video data is met by the use of Frequency Synthesizer 62 and the Voltage Controlled Oscillator 63, both of which serve to process digital input and output analog output to the receiving unit 46 [Fig. 4].

Hamlin does not disclose the YCrCb to RGB format conversion within the data routers (interface pods), nor does he disclose the ability to transmit monochrome and color video.

Filor et al disclose a system that utilizes a CSC (color space conversion) from YCrCb to RGB for further processing of the video image [col. 14, lines 5-15].

While Hamlin does not disclose the ability to transmit monochrome and color video within the system, the examiner gives Official Notice that the steps of transmitting monochrome video data and color video data are notoriously well known in the art.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the conversion from YCrCb to RGB into the interface pods and the ability to transmit monochrome and color video, in order to allow for

further processing of the video signal and for more advanced options for customizing and processing the displayed signal.

4. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamlin US patent 5,574,964, cited by examiner.

Regarding claim 18, the claimed apparatus for providing a video signal to a video display from a selectable subset of a plurality of digital video data carried on a plurality of video data channels, wherein the digital video data is generated from video signals from a plurality of video sources, and each video channel selectably carries either color or monochrome video data is met as follows:

Hamlin discloses all of the following:

- The claimed means for interpreting display commands that select a subset of the video data is met by the CPU 43 of the system controller [Fig. 3].
- The claimed means for selecting digital video data from a subset of the channels responsive to the display commands, whereby selected digital video data is provided at the output ports is met by the converter 34 [Fig. 2], which serves to input a plurality of signals and convert them so as to make them accessible on communication bus 36.
- The claimed means for merging the selected video data into frames of video data is met by the Frequency Synthesizer 62 and the Controller/Demodulator 60, which both serve to sequence the content

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delivered on the bus into frames for conversion or viewing of analog output by the receiving unit 46.

- The claimed means for converting the video data to an analog video signal from the frames of video data is met by the Frequency Synthesizer 62 and the Voltage Controlled Oscillator 63, both of which serve to process digital input and output analog output to the receiving unit 46 [Fig. 4].

While Hamlin does not disclose the ability to transmit monochrome and color video within the system, the examiner gives Official Notice that the steps of transmitting monochrome video data and color video data are notoriously well known in the art.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the ability to process both color and monochrome data, in order to allow for further processing of the video signal and for more advanced options for customizing and processing the displayed signal.

5. Claim 2-4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamlin US patent 5,574,964, cited by examiner, in view of Filor et al US patent 5,844,609, cited by examiner, in further view of Lewis US patent 5,638,426, cited by examiner.

Regarding claim 2, Hamlin and Filor teach all of that which is discussed above with regards to claim 1. Neither Hamlin nor Filor disclose that the data router is configurable to compress the input video data at selectable compression

level. Lewis discloses data that can be compressed interactively according to the users selection of a compression rate [col. 10, lines 36-43]. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize a user-selectable compression ratio, in order to interactively determine the quality of the multimedia information and the speed of transmission and therefore bandwidth used.

Regarding claim 3, Hamlin and Filor teach all of that which is discussed above with regards to claim 1. Neither Hamlin nor Filor disclose that video data is logically segmented into frames of pixel data, and the data routers are configurable for operation in a first mode or a second mode, wherein a single data router processes video data from a single channel of video data while operating in the first mode (met by the discussion of normal compression in the interface pods and transmission schemes of Hamlin), and in the second mode a first data router processes a first half of the pixel data of a frame and a second data router processes a second half of the pixel data of the frame. The aforementioned second mode is met by Lewis, wherein he discloses a system for separating the digital file into primary and secondary layers for compression and transmission [col. 11, lines 50-55]. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the mode of operation wherein two routers are used to compress a digital file, in order to alleviate stress on one router and to allow the system more flexibility in allotting responsibility for the allocation of jobs and the use of system resources and bandwidth.

Regarding claim 4, Hamlin, Filor, and Lewis disclose all of that which is discussed above with regards to claim 3. They do not, however, disclose that the compression level is selectable. Lewis discloses data that can be compressed interactively according to the users selection of a compression rate [col. 10, lines 36-43]. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize a user-selectable compression ratio, in order to interactively determine the quality of the multimedia information and the speed of transmission and therefore bandwidth used.

Regarding claim 14, Hamlin and Filor teach all of that which is discussed above with regards to claim 13. Neither Hamlin nor Filor disclose that the data router is configurable to compress the input video data at selectable compression level. Lewis discloses data that can be compressed interactively according to the users selection of a compression rate [col. 10, lines 36-43]. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize a user-selectable compression ratio, in order to interactively determine the quality of the multimedia information and the speed of transmission and therefore bandwidth used.

6. Claims 6-9 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamlin US patent 5,574,964, cited by examiner, in view of Filor et al US patent 5,844,609, cited by examiner, in further view of Coutinho et al US patent 5,808,659, cited by examiner.

Regarding claim 6, The Hamlin and Filor references teach all of that which is discussed above with regards to claim 1. Hamlin and Filor do not, however, discuss the use graphics overlay circuitry, as is discussed below with reference to Coutinho. Coutinho does disclose the following:

- The claimed first memory coupled to the processor and arranged for storage of graphics data to be overlaid on the video data is met by the PIP Display Buffer 34 [Fig. 2], which serves to store graphics and image information for use as an overlay on the main video image.
- The claimed second memory coupled to the sequencer and arranged for storage of the video data is met by the Service Driver 24 and Sampler 32, which serve to store the video data that will be mixed with the PIP Display Buffer at the Video Switch 38 [Fig. 2].
- The claimed pixel selector having input ports coupled to the first memory and to the second memory and an output port coupled to the digital-to-analog converter, wherein the pixel selector is configured and arranged to select graphics data from the first memory when graphics data is present is met by the Video Switch 38, which serves to mix the PIP Display with the Video Data from the Service Driver [Fig. 2].

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the Picture-in-Picture system as discussed, in order to allow a user to view multiple programs at once for easy viewing and channel surfing capabilities.

Regarding claim 7, Hamlin, Filor, and Coutinho teach all of that which is discussed above. Neither Hamlin nor Filor teach the idea of a third memory and pixel output controller. Coutinho, however, further discloses the following:

- The claimed third memory coupled to the processor and arranged for storage of a first-level priority graphics data is met by the Video Switch 38, which contains a third memory device for the storage of the combined display or first-level priority graphics.
- The claimed pixel output controller coupled to the third memory and to the video memory, the pixel output controller configured and arranged to sequence output of data from the first and second memories to the pixel selector and sequence first-level priority graphics data from the third memory to the digital-to-analog converter, wherein the first-level priority graphics data which takes precedence for display over the graphics data of the first memory and over the video data is met by the Video Switch 38, again, which serves to output the combined graphics data and video data in a overlaid form to the D/A Converter and Display Device.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a third memory to combine the first-level priority graphics, in order to store and therefore send the data to the D/A Converter. This process of store and forward is well known and commonly used when merging data.

Regarding claim 8, Hamlin, Filor, and Coutinho teach all of that which is discussed above. Neither Hamlin nor Filor teach the idea of a window position value. Coutinho, however, further discloses the following:

- The claimed pixel output controller being further configured and arranged to sequence output of video data from the second memory responsive to window position parameters associated with data from the video sources is met by the discussion of the PIP window placement [col. 5, lines 42-63], wherein, the placement and position of the PIP is discussed with reference to the main video data

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the video data to determine the PIP window location, in order to allow the video provider the ability to define where the PIP window resides on the screen.

Regarding claim 9, Hamlin, Filor, and Coutinho teach all of that which is discussed above. Neither Hamlin nor Filor teach the idea of a blink-translation circuit. Coutinho, however, further discloses the following:

- The claimed blink-translation circuit coupled to the first memory and to the pixel selector, wherein the blink-translation circuit is configured and arranged to selectively replace an input pixel value with a configurable pixel value at a configurable interval is met by the discussion of how the pixel values are replaced within the Video Switch 38 [col. 5, lines 42-63].

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize a blink-translation circuit, in order to allow the device to recognize what pixels should be replaced and what they should be replaced with, in order to form the PIP window overlaid on the main video data.

Regarding claim 16, Hamlin and Filor teach all of that which is discussed above with regards to claim 13. They do not, however, disclose the steps of storing video data in a first memory, storing overlay data in a second memory, and selecting between the overlay data and the video data for conversion to a video signal. Coutinho et al teach the following:

- The claimed step of storing the video data in a first memory is met by the Service Driver 24 and Sampler 32, which serve to store the video data that will be mixed with the PIP Display Buffer at the Video Switch 38 [Fig. 2].
- The claimed step of storing the overlay data in a second memory is met by the PIP Display Buffer 34 [Fig. 2], which serves to store graphics and image information for use as an overlay on the main video image.
- The claimed step of selecting between the overlay data and the video data for conversion to a video signal is met by the Video Switch 38, which serves to mix the PIP Display with the Video Data from the Service Driver [Fig. 2].

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the Picture-in-Picture system as discussed, in order to allow a

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user to view multiple programs at once for easy viewing and channel surfing capabilities.

7. Claim 10-12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamlin US patent 5,574,964, cited by examiner, in view of Filor et al US patent 5,844,609, cited by examiner, in further view of Coutinho et al US patent 5,808,659, cited by examiner, and in further view of Lewis US patent 5,638,426, cited by examiner.

Regarding claim 10, Hamlin, Filor, and Coutinho disclose all of that which is discussed above with regards to claim 6. They do not, however, disclose that the compression level is selectable. Lewis discloses data that can be compressed interactively according to the users selection of a compression rate [col. 10, lines 36-43]. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize a user-selectable compression ratio, in order to interactively determine the quality of the multimedia information and the speed of transmission and therefore bandwidth used.

Regarding claim 11, Hamlin, Filor, and Coutinho teach all of that which is discussed above with regards to claim 6. Neither Hamlin, Filor, nor Coutinho disclose that video data is logically segmented into frames of pixel data, and the data routers are configurable for operation in a first mode or a second mode, wherein a single data router processes video data from a single channel of video data while operating in the first mode (met by the discussion of normal compression in the interface pods and transmission schemes of Hamlin), and in

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the second mode a first data router processes a first half of the pixel data of a frame and a second data router processes a second half of the pixel data of the frame. The aforementioned second mode is met by Lewis, wherein he discloses a system for separating the digital file into primary and secondary layers for compression and transmission [col. 11, lines 50-55]. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the mode of operation wherein two routers are used to compress a digital file, in order to alleviate stress on one router and to allow the system more flexibility in allotting responsibility for the allocation of jobs and the use of system resources and bandwidth.

Regarding claim 12, Hamlin, Filor, Coutinho, and Lewis disclose all of that which is discussed above with regards to claim 10. They do not, however, disclose that the compression level is selectable. Lewis discloses data that can be compressed interactively according to the users selection of a compression rate [col. 10, lines 36-43]. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize a user-selectable compression ratio, in order to interactively determine the quality of the multimedia information and the speed of transmission and therefore bandwidth used.

8. Claim 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamlin US patent 5,574,964, cited by examiner, in view of Filor et al US patent 5,844,609, cited by examiner, in further view of Lewis US patent 5,638,426, cited by examiner, and in further view of Coutinho et al US patent 5,808,659, cited by examiner.

Regarding claim 15, Hamlin, Filor, and Lewis teach all of that which is discussed above with regards to claim 14. They do not, however, disclose the steps of storing video data in a first memory, storing overlay data in a second memory, and selecting between the overlay data and the video data for conversion to a video signal. Coutinho et al teach the following:

- The claimed step of storing the video data in a first memory is met by the Service Driver 24 and Sampler 32, which serve to store the video data that will be mixed with the PIP Display Buffer at the Video Switch 38 [Fig. 2].
- The claimed step of storing the overlay data in a second memory is met by the PIP Display Buffer 34 [Fig. 2], which serves to store graphics and image information for use as an overlay on the main video image.
- The claimed step of selecting between the overlay data and the video data for conversion to a video signal is met by the Video Switch 38, which serves to mix the PIP Display with the Video Data from the Service Driver [Fig. 2].

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the Picture-in-Picture system as discussed, in order to allow a user to view multiple programs at once for easy viewing and channel surfing capabilities.

Regarding claim 17, Hamlin, Filor, and Lewis teach all of that which is discussed above with regards to claim 13. They do not, however, disclose steps

of establishing and selecting priority levels and pixel display ability, as is discussed in this claim. Coutinho et al teach the following:

- The claimed step of establishing respective priority levels for the digital video data generated from the video signals from the video sources is met by the ability for the video switch to utilize the pixel numbers and position characteristics in order to replace certain pixels with pixel information from the PIP display buffer 34 [col. 6, lines 1-15].
- The claimed step of selecting between the portion of the video data from the first channel and the portion of the video data from the second channel responsive to the priority levels, if a portion of the selected video data from a first one of the subset of channels and a portion of the selected video data from a second one of the subset of channels require common storage space in the first memory is met by the video switch and it's ability to select image information based on pixel number to combine the full screen image and the PIP image for output to the display device [col. 6, lines 1-15].

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the Picture-in-Picture system as discussed, in order to allow a user to view multiple programs at once for easy viewing and channel surfing capabilities.

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Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael R Shannon whose telephone number is 703-305-6955. The examiner can normally be reached on M-F 7:30-5:00, alternate Friday's off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on 703-305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael R Shannon
Examiner
Art Unit 2614

Michael R Shannon
January 6, 2005


JOHN MILLER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600